Mummana Jagadeesh

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Education

B.Tech, Electronics and Communication Engineering *Graduating May 2027*
National Institute of Technology Calicut, KERALA 8.51/10 (SEM 6)

Relevant Coursework: Digital Electronics, Semiconductor Physics, HDLs, VLSI Digital Design, VLSI Design Automation, VLSI Testing, Hardware Architectures for Deep Neural Networks, Computer Architecture, GPU Architectures and Programming, Data Converters

Skills & Familiar Tools

Core Interests	Digital Design & Verification, Computer Architecture, Physical Design, Open-Source Hardware
Hardware Design	RTL, CMOS, FSMs, Verilog/SystemVerilog (basic), SVA, FPGAs
EDA (Industry)	Cadence (Genus, Virtuoso), Xilinx Vivado, ModelSim, Quartus Prime, LTSpice
EDA (Open-Source)	OpenLane, Icarus, Yosys/SymbiYosys, cocotb, Magic VLSI, NgSpice
Programming & Automation	Python, C/C++, MATLAB; Linux, Git/Github, Docker, TCL; LaTeX

Projects

Low-Power 5-Port Wormhole Router | *Scan Chains* | *Timing closure*

- Designed a 5-port wormhole router with dual-VC FIFOs implemented in OpenRAM SRAM macros and XY routing
- Reduced power 70.34% through clock gating, isolation, synthesis tuning, CTS tuning, and floorplan changes
- Added pipelining and macro-aware placement; setup slack improved 13.4% and die area dropped 16.47%.
- Built custom OpenLane2 scan-insertion automation (720 FFs/4 chains) & ran submodule gate-level ATPG (98.1% coverage)

Pipelined Systolic Array-Based GEMM/CONV Microarch | *Digital Design* | *PPA Evaluation*

- Designed output-stationary (M+N-1)-stage PE array for 8-bit GEMM; im2col Conv2D wrapper with 99.5% burst efficiency
- MAC physical design sweep of 9 sky130A variants; identified Booth+RCA for min area, Array+Kogge for max Fmax
- Evaluated caching strategies (direct-mapped, SA, FA); proved 2-way SA doubles DM hit rate at 26% gate overhead

INT8 Fixed-Point CNN Hardware Accelerator and Image-Processing Suite | *Digital Electronics* | *Open-Source EDA*

- Designed a shallow 2-block Res-CNN for CIFAR-10 balancing accuracy (83%), FLOPs (12.6M) & memory (52KB)
- Implemented tiling based Conv core; AXI4-Lite weight cfg, AXI-Stream image via DDR-DMA; TB-verified
- Applied PTQ/QAT (Q1.7); achieved 4× memory reduction with <1% acc. loss; validated TF FP32–RTL consistency
- Automated TCL/Py inference/ROM gen; AXI-Stream DIP toolkit (encode/edge/filter) with FIFO backpressure handling

Design & Formal Verification of Parameterized Fixed-Point CORDIC IP | *IP Design* | *SVA* | *DSP*

- Implemented parameterized shift-add datapath supporting circular/linear/hyperbolic (rotation/vectoring modes)
- Designed basic math wrappers; observed ∼4e-5 RMS at baseline (32b, 16 iter); core packaged via FuseSoc
- Formally verified core via SVAs (SymbiYosys): deadlock-free progress, monotonicity, range safety; Py-automated ROM gen
- Variants: pipelined/SIMD/multi-issue; Systems: 16-QAM demod (Costas, Gardner), DPLL, ΣΔ-ADC FE, FFT/IFFT

Dual-Issue Superscalar RV32I CPU: Design, Verification, and Performance Evaluation | *Computer Architecture*

- Built 2-wide in-order with dual 5-stage, 4R2W regfile, inter-lane RAW/WAW, branch squash + slot-1 suppress
- Optimizations: ID-stage branch resolve, MEM→EX forward, LU elimination; CPI 1.31→1.06 (pipe), 1.04→0.72 (SS)
- Branch prediction study: static/1-bit/2-bit/global, hybrid tournament, BTB & RAS; prototyped Tomasulo-style OoO
- RV32I(M) design (SC/MC, 3/5/7-stages, superscalar); CoreMark/MHz via perf ctrs; RISCOF-ACT; C vs Spike/QEMU

Fixed-Point Rasterizer with SIMD Extension: Design and Functional Verification | *SystemVerilog* | *Verification*

- 12-opcode cmd-decoded triangle setup: vertex/color load, framebuffer clr, fog config; fixed-point edges & AABB clamp
- Scanline rasterizer: incremental edge walk, FIFO decoupling, 2-stage barycentric interp, fog blend; Py painter-sort 3D scene prep
- SIMD 8-lane warp extension: parallel interp/shader, single-cycle 8-port FB write; 7.7x throughput (0.50→3.86 px/cyc)
- Constrained-rand SV/Py TB: golden vs scoreboard, cmd-protocol/FIFO/pixel-conservation checks, 14-bin coverage & regressions

Lab/Research Involvement

Research Intern (Supervisor: Dr. Ayan Palchaudhuri)
Chip Design Simulation Lab, IIT Bhubaneswar *May 2026 – Jul 2026*
Publication: *Comparative Hardware and Statistical Evaluation of LFSR-Derived and Cellular Automaton Structures for Pseudo-Random Pattern Generation in BIST (in preparation, target: IEEE TVLSI/TCAD)*

- Compared 9 PRNG architectures spanning LFSR variants and cellular automata across hardware and randomness metrics
- Proposed 2 novel intermediate architectures bridging LFSR and CA designs with tunable hardware–randomness tradeoffs
- Optimized FPGA implementations via SRL inference, LUT6_2 packing, and placement-constrained column layouts
- Investigated ASIC optimizations through XOR reduction, logic sharing, fanout management, and synthesis-driven timing
- Evaluated 81 seed–architecture combinations using NIST, correlation, entropy, and ISCAS-85 fault coverage analyses
- Automated RTL generation and cross-variant evaluation via a packaged Python CLI tool; co-authoring the publication

Technical Team Head, Robotics Interest Group
Mechatronics Lab, NIT Calicut *Nov 2024 – Present*

- Circuit design and sensor fusion for institute-funded projects; led competition teams & co-org ORIGO workshops and lab visits
- Computer vision and sim-based perception/nav verification (Simulation-Team Head); maintained website, codebase & tech blog

Achievements

1st Prize (National) | RV32I RISCV CPU on Spartan-7 | HackS'US-V CarbonX (RSET IEDC & C-DAC)

- Designed RV32I cores (SC, MC, 5-stage pipeline, dual-issue superscalar); compared CPI/IPC/latency/LUTs & demonstrated on FPGA

FIR Accelerator SoC Proposal Accepted | μW Momentum – OpenPOWER HW Design International Hackathon

- Proposed parameterizable FIR accelerator SoC; selected for potential fab via ChipFoundry & Google/Efabless OpenMPW shuttle
- Integrated CIC decimator, 8-tap FIR, PWM DAC in Caravel SoC; Wishbone-controlled with runtime-programmable Q1.15 coeffs

Certified Top Performer (Analog Track) | Texas Instruments – TI BYTE Program *May – Jul 2025*

- Analog electronics fundamentals, including circuit analysis, & hands-on simulation exercises

Samsung Fellowship (Grade I) | ISWDP – IISc, Synopsys & Samsung *Jun – Sep 2025*

- Semiconductor physics, TCAD device modeling (Sentaurus TCAD), & fab process fundamentals

Electronic Circuit Design & Debugging – 2× Winner & National Finalist | IITM, NITT, NITC Technical Fests

- IITM Shastra'26 (ACDC, Finals); NITT Probe'25 (DCDC, Finals); NITC Tathva (Circuit Conclave'24/25 1st/3rd; Disarmamine'24 3rd)

Challenges & Open-Source

Hardware-Accelerated CNN on FPGA (Zynq7000) (Bharat AI SoC Challenge'26 by ARM & C2S India)

- Designed Vitis HLS CNN with AXI/DDR interfaces; reduced LUTs by 74% (70k→18.3k) through pointer-index optimization
- Achieved 136 MHz at 34% LUT/86% BRAM/10% DSP usage; validated alternative deployment flows with Brevitas QAT and FINN
- Benchmarked ARM Cortex-A9 (QEMU) SW baselines, integrated HLS IP in Vivado BD, and achieved 5.26× inference speedup

UVM & Functional Verification of 2nd-Order Digital PLL (TinyTapeout)

- Fully-synchronous DPLL: CORDIC NCO, cross-product PD (Q2.30), PI filter + anti-windup; pull-in to 0.040 rad/sample
- 4-method verif: Python golden (acq, lock time, phase 0°–180°, SS err <1e-7); cocotb; pyuvm; SymbiYosys formal
- RTL2GDS via OpenLane: Yosys pre-eval, 68.2% util, CTS, zero-DRC routing, STA across 9 PVT corners
- 6 fixed-point bugs isolated analytically: 32×32 truncation, Q2.28 MUL_SH, `adj_valid` race, integrator windup

FPGA-Based Autonomous Maze Solver Bot (IITB eYRC'26) [Rank 13]

- Implemented FSM motion ctrl with multi-sensor fusion (US/IR/Temp/Moist), encoder feedback, & limit-switch collision recovery
- Built quadrature decoders, PWM motor/servo controllers, & UART RX/TX; validated via calibration and maze-run benchmarks

Mathematical Modeling of Pipelined ADC (TI Design Contest'26)

- Modeled 5+4 bit pipelined ADC; used 1-bit redundancy to correct flash offsets; recovered ENOB from ∼4 to 7.8 bits
- Implemented PRBS-based background calibration to estimate & compensate 5% inter-stage gain errors via correlation logic
- Verified DEC/Calibration via FFT (SNDR/SFDR) and transfer curves; eliminated sparkle codes and sub-range glitches

Global Placement Optimization (Macro Placement Challenge'26 by Partcl and HRT) [Rank 50]

- Legality-aware macro placer via smooth WL + neighborhood search; avg proxy 1.3241, beating RePlAce & SA on IBM benchmarks

Autonomous Drone for GNSS-Denied Environments (ISRO IRoC-U'25) [Top 24 Teams]

- Integrated Jetson Nano & Pixhawk 4; interfaced (barometer/optical-flow/stereo vision) for fused state estimation
- Worked with ESP32 telem (500 m) & safe zone detection; VIO ROS2 (VINS-Fusion); validated in Mars-like Webots sim

AWS AI/ML Student League'24: Fine-tuned PPO-RL models for autonomous driving (AWS SageMaker, DeepRacer) **Global Leaderboard**

Leadership & Activities

Mentor - RIGNITC; Reliance Foundation | **Volunteer** - IPR Plasma Exhib; NASA IASC | **Treasurer** - ECEA | **Outreach** - Tech Conclave