Mummana Jagadeesh

+91-7569664234 mummanajagadeesh97@gmail.com
github.com/mummanajagadeesh linkedin.com/in/jagadeesh-mummana mummanajagadeesh.github.io

Education

B.Tech, Electronics and Communication Engineering Graduating May 2027
National Institute of Technology Calicut, KERALA 8.6/10 (SEM 4)

Minor in Robotics and Automation (2024-2025)

Relevant Coursework: Digital Electronics, Semiconductor Physics, Intro to HDLs, VLSI Digital Design, VLSI Testing, Analog Circuits, Computer Architecture, Embedded Systems, Foundations of ML, DSA, Design with OpAmps & Analog ICs, Data Conversion Systems
PG Courses: Hardware Architectures for Deep Neural Networks, VLSI Design Automation

Projects

INT8 Fixed-Point CNN Hardware Accelerator and Image-Processing Suite / *Verilog* / *Digital Electronics* / *Open-Source EDA* **Link**

- Designed a synthesizable shallow Res-CNN for CIFAR-10, Pareto-optimal among 8 CNNs for throughput, latency, and accuracy
- Built systolic-array PEs with 8-bit CSA–MBE MACs, FSM-based control, 2-cycle read/valid handshake, and verified TB operation
- Performed PTQ/QAT (Q1.31→Q1.3) analysis; Q1.7 PTQ retained ∼84% accuracy (<1% loss) with 4x smaller (∼52kB) memory footprint
- Auto-generated 14 coeff & 3 RGB ROMs via TCL/Py automation; validated TF/FP32–RTL consistency and automated inference execution
- Implemented digital image-processing toolkit (edge, denoise, filter, enhance) & MLP classifier on (E)MNIST (>75% acc.) with GUI viz

3-Stage Pipelined Systolic Array-Based MAC Microarchitecture / *Digital Design* / *PPA Evaluation*

- Benchmarked six 8-bit signed adders-multipliers via identical RTL2GDS Sky130 flow to isolate arithmetic-level post-route PPA trade-offs
- 3-stage pipelined systolic MAC (CSA-MBE), achieving ↓66.3% delay; ↑3.1× area efficiency; ↓82.2% typical power vs naïve conv3 baseline
- Used a 2D PE-grid structure for convolution (verified 0/same padding modes) and optimized GEMM (reducing power by 44.6%; N = 3)
- Added a 648-bit scan chain across all pipeline/control registers, enabling full DFT/ATPG testability with only +14.5% cell overhead

FPGA-Based Maze Solver using Custom RV32I Single-Cycle CPU (IITB eYRC'26) / *FPGA* / *Architecture (Basic)*

- Built a 32-bit RISCV core (32×32 regfile); 38 ISA ops & full load/store (LB/LBU/LH/LHU/LW, SB/SH/SW), incl. RMW & sign/0 ext
- Verified RTL in ModelSim & deployed on Cyclone-IV via Quartus, with timing checks & on-chip waveform capture using SignalTap
- Implemented ultrasonic/IR/temp–humidity/soil-moisture sensing with ADC & UART telemetry via CPU-managed peripheral FSMs
- Conducted hardware testing for motor control, sensor calibration, & maze runs ensuring reliable parallel sensing & actuation on FPGA

Dual-Issue 16-bit RISC Superscalar Processor / *Architecture*

- Built a two-wide in-order superscalar RISC processor with parallel IF–ID–EX–MEM–WB lanes and independent pipeline registers per lane
- Designed dual 16-bit instruction fetch per cycle with inter-lane dependency checks, hazard suppression, and load-use stall handling
- Implemented 4R2W register file, RAW/WAW detection, branch squashing, & multi-port memory for concurrent fetch and data access
- Evaluated SC/MC/5-stage pipelined designs via directed programs, analyzing CPI (1/3.8/1.6), cycle counts, and hazard overhead

Design & Verification of Parameterizable CORDIC Core Soft IP with Trig Wrappers / *Basic IP Design*

- Implemented a synthesizable fixed-point CORDIC core (16-iter; 32-bit) with configurable width, iteration count, and shift-add datapath
- Added sin, cos, and tan wrappers using pre-scaled initial vectors, with a 16-entry atan table in Q3.29 for angle updates
- Verified using a modular angle-sweep TB against double-precision outputs, achieving 4e-5 max error (sin/cos); packaged with FuseSoC

Design & Verification of Peripheral Serial Comm Protocols (I2C/SPI/UART) / *Protocols* / *FSMs*

- Implemented synthesizable, parameterizable I2C, SPI, and UART controllers with modular interfaces and configurable timing
- I2C master: START/STOP generation, ACK/NACK handling, programmable SCL high/low periods, and clock-stretch detection
- SPI master: modes 0–3, full-duplex 8-bit transfers, adjustable SCLK division, and deterministic FSM-based shifting
- UART: simple baud generator with start/stop framing and single-byte serialization for FPGA/SoC peripheral use

Functional Verification of secworks/sha256 Core / *TCL* / *Functional Verification*

- Verified the SHA256 core using directed, random, corner-case, and negative tests to check digest correctness and multi-block behavior
- Added malformed and out-of-order sequence tests to exercise control paths and detect failure conditions
- Automated compilation, simulation, and result checking through a TCL-driven flow producing consolidated regression summaries

Pipelined ALU with Scan-Chain Integration / *Scan Chain*

- Implemented non-pipelined, pipelined, and scan-enabled versions of a 4-stage ALU, adding scan FFs in place of standard registers
- Verified scan-in, capture, and scan-out behavior and observed timing impact from scan mux insertion using fmax and path reports
- Compared delay, logic/route split, and critical-path shifts across the three versions for basic DFT and pipeline analysis

Basic Python Tool for ISCAS'85 Benchmark Analysis & Fault Modeling / *Fault Modeling* / *Automation*

- Built a tool for structural Verilog gen, random TBs, serial/parallel fault sim, FFR-based dom/eqv collapsing, and CC0/CC1/CO metrics
- Added fault dictionaries, coverage reporting, and SCOAP-based ATPG with a developing PODEM-style search

Achievements

Certified Top Performer in TI BYTE | Build Your Tech Edge Program by Texas Instruments (Analog)
- 2-month up-skilling program focused on analog electronics fundamentals, including circuit analysis, and hands-on simulation exercises

Samsung Fellowship (Grade I) | Indian Semiconductor Workforce Development Program (ISWDP; IISc, Synopsys & Samsung)
- 3-month program (1, 2, Adv levels) focused on semiconductor physics, TCAD device modeling, & fab process fundamentals

FIR Accelerator SoC Proposal Accepted | Microwatt Momentum (OpenPOWER HW Design International Hackathon)
- Proposed parameterizable FIR accelerator SoC; selected for potential fab via ChipFoundry & Google/Efabless OpenMPW shuttle

Winners (2x Consecutive Years) | Electronics Design Events, Tathva Annual Tech Fest, NITC
- Circuit Conclave (Tathva'24: 1st; Tathva'25: 3rd), Disarmamine (Tathva'24: 3rd); digital/analog circuit design and debugging events

Skills & Familiar Tools

Core Interests	Digital Design, Verification, Analog/Mixed-Signal Circuits
Hardware Design	RTL, FSMs, CMOS, FPGAs, ADC/DAC basics
HDL & Programming	Verilog HDL, SystemVerilog (basics), Python, C/C++, MATLAB
Industry EDA	Xilinx Vivado, ModelSim, Quartus Prime, Cadence Virtuoso
OpenSource EDA	Icarus Verilog, Yosys, OpenLane, Magic VLSI
Microcontrollers	8051, MSP430, AVR/Arduino, ESP32/8266, Proteus
Automation & Workflow	Linux, Git, GitHub, Docker, Make, TCL, Bash, LaTeX
Mixed-Signal Simulation	LTspice, Ngspice, Xyce, Qucs-S, Xschem

Lab Involvement

Technical Team Member
Robotics Interest Group NIT Calicut | Robotics Club, Mechatronics Lab Nov 2024 – Present
- Designed & integrated sensor/power/control electronics for institute-funded projects, improving system reliability and accuracy
- Developed on-board interfaces & multi-sensor fusion for navigation/perception logic; led sim-driven verification as Simulation-Team Head
- Led robotics competition teams & mentored juniors; showcased projects in lab visits & co-organized ORIGO workshops (200+ participants)
- Managed shared codebases/docs & CI workflows; built and maintained the club's official website & technical blog as Web-Team Lead
- **Competitions: e-Yantra eYRC (FPGA-based Maze Solver Robot); ISRO IRoC-U 2025 (GPS-denied Autonomous Drone)**

Other Achievements & Roles

Ranked Top 24 in India | ISRO National Robotics Challenge (IRoC-U 2025) | Eliminations Round
- Built an autonomous drone for GNSS-denied environments, aimed at navigation and mapping of Martian surface zones

Top Global Rank | AWS AI/ML Global Student League (Udacity & AWS Scholarship Program)
- Fine-tuned PPO-based RL models on AWS SageMaker for autonomous driving on AWS DeepRacer, achieving sub-2-minute laps

Mentor - RIGNITC; Reliance Foundation | **Volunteer** - IPR Plasma Exhib; NASA IASC | **Executive** - ECEA | **Outreach** - Tech Conclave

Other Domain Projects

Autonomous Drone for GNSS-Denied Environments (ISRO IRoC-U 2025) / *Sensor Interfacing* / *Robotics* **Link**
- Integrated NVIDIA Jetson Nano (on-board compute) & Pixhawk 4 (flight controller) for autonomous navigation and precision landing
- Designed sub-2 kg quadrotor optimized for GNSS-denied mapping, localization, and vision-based safe-zone detection
- Calibrated ESCs and configured 5 V 3 A BEC for stable power; established bidirectional telemetry via ESP32 ($\sim$500 m range)
- Interfaced barometer, optical-flow, and stereo-vision sensors with Pixhawk over I2C/UART for fused state estimation
- Implemented visual-intertial odometry using ORB-SLAM3 and VINS-Fusion (ROS 2), achieving $\sim$5 m localization with $<$5 cm drift
- Simulated Mars-like no-GPS flights in Webots (0.38 g gravity), enabling autonomous landings within 1.5 m $\times$ 1.5 m safe zones

Project Member
ECED, NIT Calicut | Under Dr. Sudhish N George, NIT Calicut Mar 2025 – Jun 2025

Contributed to a Ph.D. supervised project on MRI-based Alzheimer's and MCI classification, designed 3D CNNs in PyTorch/MONAI with Med3DNet backbones, DICOM/NIfTI preprocessing (radiomic feat, voxel norm), and Bayesian-tuned 3D convolutions achieving >93% acc.

up-to-date version of this document can be found at:
mummanajagadeesh.github.io/resume/