Mummana Jagadeesh

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Education

B.Tech, Electronics and Communication Engineering *Graduating May 2027*
National Institute of Technology Calicut, KERALA 8.6/10 (SEM 5)

Relevant Coursework: Digital Electronics, Semiconductor Physics, HDLs, VLSI Digital Design, VLSI Design Automation, VLSI Testing, Hardware Architectures for Deep Neural Networks, Computer Architecture, Data Converters

Skills & Familiar Tools

Core Interests	Digital Design & Verification, Computer Architecture, Physical Design, Open-Source Hardware
Hardware Design	RTL, CMOS, FSMs, Verilog/SystemVerilog (basic), TB, SVA, FPGAs
EDA (Industry)	Cadence (Genus, Virtuoso), Xilinx Vivado, ModelSim, Quartus Prime, LTSpice
EDA (Open-Source)	Icarus, Yosys/SymbiYosys, OpenLane, OpenSTA, Bambu HLS, Magic VLSI, NgSpice
Programming & Automation	Python, C/C++, MATLAB; Linux, Git/GitHub, Docker, Perl/TCL; LaTeX

Projects

INT8 Fixed-Point CNN Hardware Accelerator and Image-Processing Suite | *Digital Electronics* | *Open-Source EDA*

- Designed a shallow 2-block Res-CNN for CIFAR-10 balancing accuracy (83%), FLOPs (12.6M) & memory (52KB)
- Implemented systolic-array based Conv core; AXI4-Lite weight cfg, AXI-Stream image via DDR-DMA; TB-verified
- Applied PTQ/QAT (Q1.7); achieved 4× memory reduction with <1% acc. loss; validated TF FP32–RTL consistency
- Automated TCL/Py inference/ROM gen; AXI-Stream DIP toolkit (encode/edge/filter) with FIFO backpressure handling

Design & Formal Verification of Parameterized Fixed-Point CORDIC IP | *IP Design* | *SVA* | *DSP*

- Implemented parameterized shift-add datapath supporting circular/linear/hyperbolic (rotation/vectoring modes)
- Designed basic math wrappers; observed ∼4e-5 RMS at baseline (32b, 16 iter); core packaged via FuseSoc
- Formally verified core via SVAs (SymbiYosys): deadlock-free progress, monotonicity, range safety; Py-automated ROM gen
- Variants: pipelined/SIMD/multi-issue; Systems: 16-QAM demod (Costas, Gardner), DPLL, ΣΔ-ADC FE, FFT/IFFT

Pipelined ALU with Scan-Chain Integration | *Scan Chains* | *Timing closure*

- Designed 4-stage ALU (non-pipe, pipe, scan, dual-scan) with scan FF replacement
- Achieved ∼1.7× fmax via pipelining; Sky130 gate-level STA (Yosys/OpenSTA) with clk uncertainty & I/O delays
- Executed RTL2GDS studies (scan vs no-scan, CTS skew, floorplan stress) with timing closure; clk-gating ↓ switching power ∼19%
- IO-driven routing & PDN: worst-case pinning → >2× clk WL; pin-arch opt (>50% WL ↓); CDC via async FIFO + 2FF sync

Dual-Issue Superscalar RV32I CPU: Design, Verification, and Performance Evaluation | *Computer Architecture*

- 2-wide in-order with dual 5-stage, 4R2W regfile, inter-lane RAW/WAW, LU stalls, branch squash + slot-1 suppress
- Optimizations: ID-stage branch resolve, MEM→EX forward, LU elimination; CPI 1.31→1.06 (pipe), 1.04→0.72 (SS)
- Branch prediction study: static/1-bit/2-bit/global, hybrid tournament, BTB & RAS; prototyped Tomasulo-style OoO
- Design of SC/MC/5-stage RV32I(M), CoreMark/MHz eval via perf ctrs; verified via RISCOF-ACT, C vs Spike/QEMU

Pipelined Systolic Array-Based GEMM/CONV Microarch | *Digital Design* | *PPA Evaluation*

- (M+N-1)-stage PE array (Booth/Kogge); 9 MAC variants PPA-benchmarked; Sky130 OpenLane hardened; func verified
- im2col Conv2D on 2D PE-array; 42.47 MAC-ops/cyc (99.5% of peak @66.3% PE util), 4x16x36 output-stationary
- Ping-pong SRAM tiled GEMM (overlap load/compute, 1-cyc swap); direct-mapped tile cache (tag+valid, DMA) at 93.75% hit-rate

Parameterizable AHB-APB Bridge with Self-Checking Verification | *SystemVerilog* | *Protocols*

- AHB-Lite–APB bridge: FSM-controlled R/W, single & burst; pipelined + non-pipelined paths, addr/data buffering
- Self-checking SV TB: mode-controlled tests, protocol-phase assertions; plus standalone I2C/SPI/UART controllers

UVM & Functional Verification of secworks/sha256 Core | *TCL* | *Functional Verification*

- Verified via directed, random, corner-case, & negative tests; added malformed sequences and TCL-driven regression automation
- Implemented a basic SV/UVM env (agent/driver/sequencer/monitor/scoreboard), reusing existing tests for modular verif

Lab Involvement

Technical Team Head
***Robotics Interest Group*, Mechatronics Lab – NIT Calicut** *Nov 2024 – Present*

- **Electronics**: sensor/control ckt design; on-board interfaces, sensor fusion for institute-funded interdisciplinary projects
- **Robotics**: computer vision & sim-based verification of perception/nav logic (Simulation-Team Head); mentored juniors
- **Teamwork**: led competition teams; co-org ORIGO workshops and lab visits; **Maintainer**: website, shared codebase & tech blog

Achievements

1st Prize (National) | RV32I RISCV CPU on Spartan-7 | HackS'US-V CarbonX (RSET IEDC & C-DAC)
- Designed RV32I cores (SC, MC, 5-stage pipeline, dual-issue superscalar); compared CPI/IPC/latency/LUTs & demonstrated on FPGA

FIR Accelerator SoC Proposal Accepted | Microwatt Momentum – OpenPOWER HW Design International Hackathon
- Proposed parameterizable FIR accelerator SoC; selected for potential fab via ChipFoundry & Google/Efabless OpenMPW shuttle
- Integrated CIC decimator, 8-tap FIR, PWM DAC in Caravel SoC; Wishbone-controlled with runtime-programmable Q1.15 coeffs

Certified Top Performer (Analog Track) | Texas Instruments – TI BYTE Program *May – Jul 2025*
- Analog electronics fundamentals, including circuit analysis, & hands-on simulation exercises

Samsung Fellowship (Grade I) | ISWDP – IISc, Synopsys & Samsung *Jun – Sep 2025*
- Semiconductor physics, TCAD device modeling (Sentaurus TCAD), & fab process fundamentals

Electronic Circuit Design & Debugging – 2× Winner & National Finalist | IITM, NITT, NITC Technical Fests
- IITM Shastra'26 (ACDC, Finals); NITT Probe'25 (DCDC, Finals); NITC Tathva (Circuit Conclave'24/25 1st/3rd; Disarmamine'24 3rd)

Challenges & Other

Hardware-Accelerated CNN on FPGA (Zynq7000) (Bharat AI SoC Challenge'26 by ARM & C2S India)
- Vitis HLS Kernel: ↓74% LUTs (70k→18.3k) via pointer indexing; utilized 34% LUT/86% BRAM/10% DSP @136 MHz
- Achieved 22% LUT/14% BRAM/1% DSP footprint (12.6M FLOPs) via Brevitas 4-bit QAT & FINN flow
- Benchmarked PYNQ SW baselines (NumPy/keras2c) on ARM Cortex-A9; explored hls4ml IP generation within Vivado BD

FPGA-Based Autonomous Maze Solver Bot (IITB eYRC'26) **Rank 13 (India)**
- Implemented FSM motion ctrl with multi-sensor fusion (US/IR/Temp/Moist), encoder feedback, & limit-switch collision recovery
- Built quadrature decoders, PWM motor/servo controllers, & UART RX/TX; validated via calibration and maze-run benchmarks

Mathematical Modeling of Pipelined ADC (TI Design Contest'26)
- Modeled 5+4 bit pipelined ADC; used 1-bit redundancy to correct flash offsets; recovered ENOB from ∼4 to 7.8 bits
- Implemented PRBS-based background calibration to estimate & compensate 5% inter-stage gain errors via correlation logic
- Verified DEC/Calibration via FFT (SNDR/SFDR) and transfer curves; eliminated sparkle codes and sub-range glitches

EDA/ML Analysis Tools & Performance Evaluation
- **Pre-Routing Congestion Pred.**: Encoder-Decoder FCN on 14nm FinFET design features (macro-region/RUDY/pin-density)
- **Py-tool for ISCAS'85 Analysis**: structural Verilog gen, fault sim, SCOAP metrics & FFR-based dom/eqv fault collapsing
- **Branch Prediction & Cache Replacement**: MPKI/IPC analysis, global vs local history, RF/DT vs bimodal; ChampSim
- **CSR SpMV (CPU/OpenMP & GPU/CUDA)**: warp-level 2.5× DRAM BW gain, PCIe measurement & memory roofline validation

Autonomous Drone for GNSS-Denied Environments (ISRO IRoC-U'25) **Top 24 Teams (India)**
- Integrated Jetson Nano & Pixhawk 4; interfaced (barometer/optical-flow/stereo vision) for fused state estimation
- ESC calib; 5V/3A BEC & ESP32 telem (500 m); VIO ROS2 (ORB-SLAM3/VINS-Fusion); validated in Mars-like Webots sim

AWS AI/ML Student League'24: Fine-tuned PPO-RL models for autonomous driving (AWS SageMaker, DeepRacer) **Global Leaderboard**

Leadership & Activities

Mentor - RIGNITC; Reliance Foundation | **Volunteer** - IPR Plasma Exhib; NASA IASC | **Treasurer** - ECEA | **Outreach** - Tech Conclave

up-to-date version of this document can be found at:
mummanajagadeesh.github.io/resume/